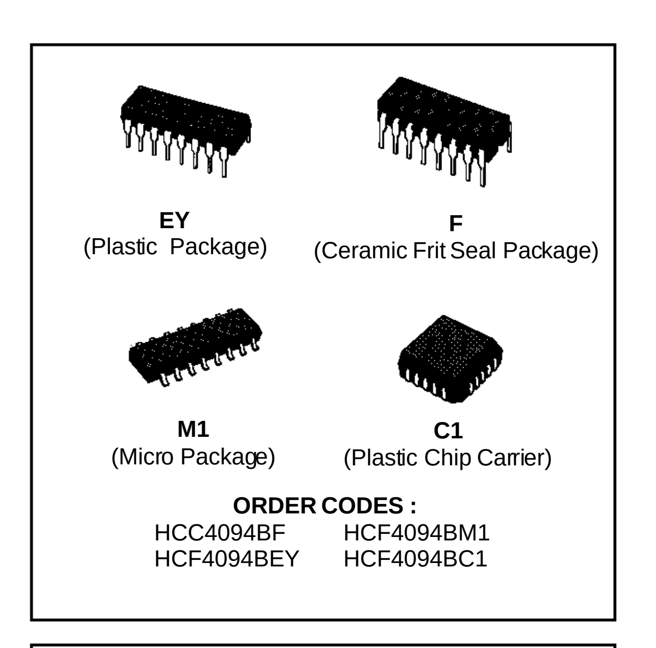


HCC/HCF4094B

8–STAGE SHIFT-AND-STORE BUS REGISTER

- 3-STATE PARALLEL OUTPUTS FOR CONNECTION TO COMMON BUS
- SEPARATE SERIAL OUTPUTS SYNCHRONOUS TO BOTH POSITIVE AND NEGATIVE CLOCK EDGES FOR CASCADING
- MEDIUM SPEED OPERATION 5MHz AT 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

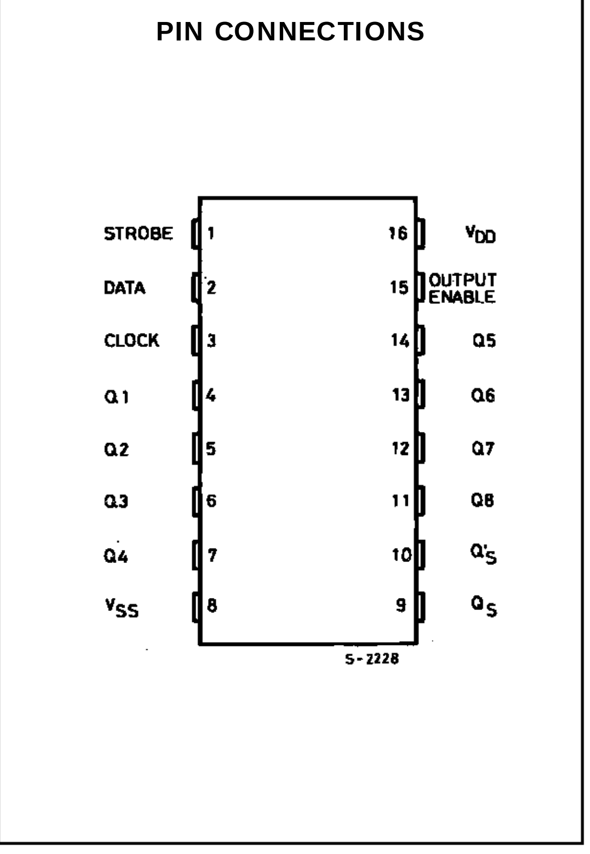


DESCRIPTION

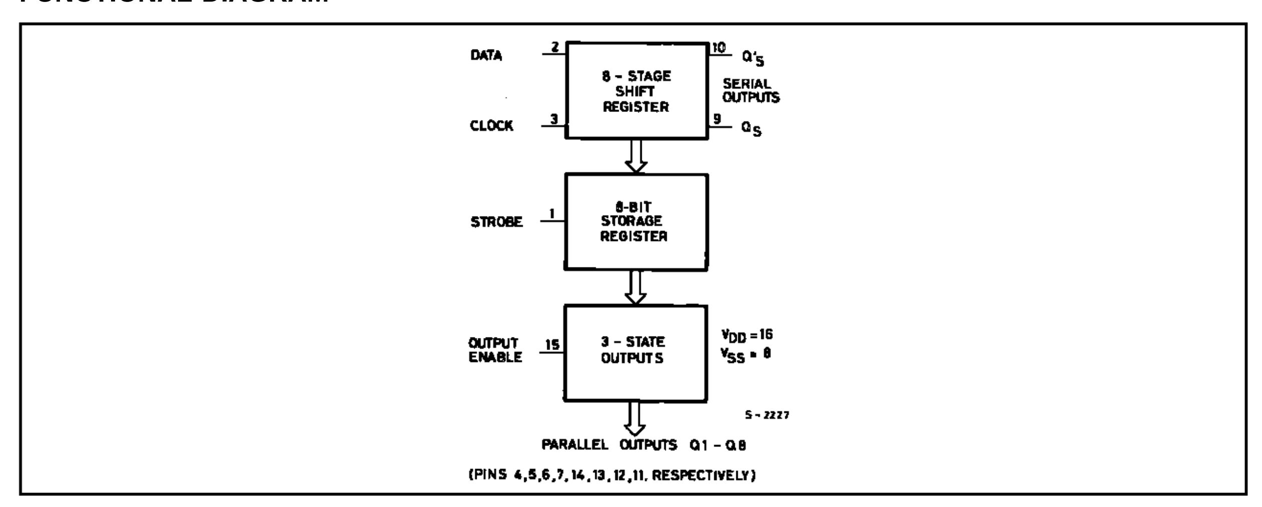
The **HCC4094B** (extended temperature range) and **HCF4094B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic packageand plastic micropackage.

The **HCC/HCF4094B** is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high. Two serial outputs are available for cascading a number of **HCC/HCF4094B** devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'_S terminal on the next negative clock edge, provides a means for cascading **HCC/HCF4094B** devices when the clock rise time is slow.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage : **HCC** Types **HCF** Types	– 0.5 to + 20 – 0.5 to + 18	V V
V_i	Input Voltage	– 0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for T_{op} = Full Package-temperature Range	200 100	mW mW
T_{op}	Operating Temperature : **HCC** Types **HCF** Types	– 55 to + 125 – 40 to + 85	°C °C
T_{stg}	Storage Temperature	– 65 to + 150	°C

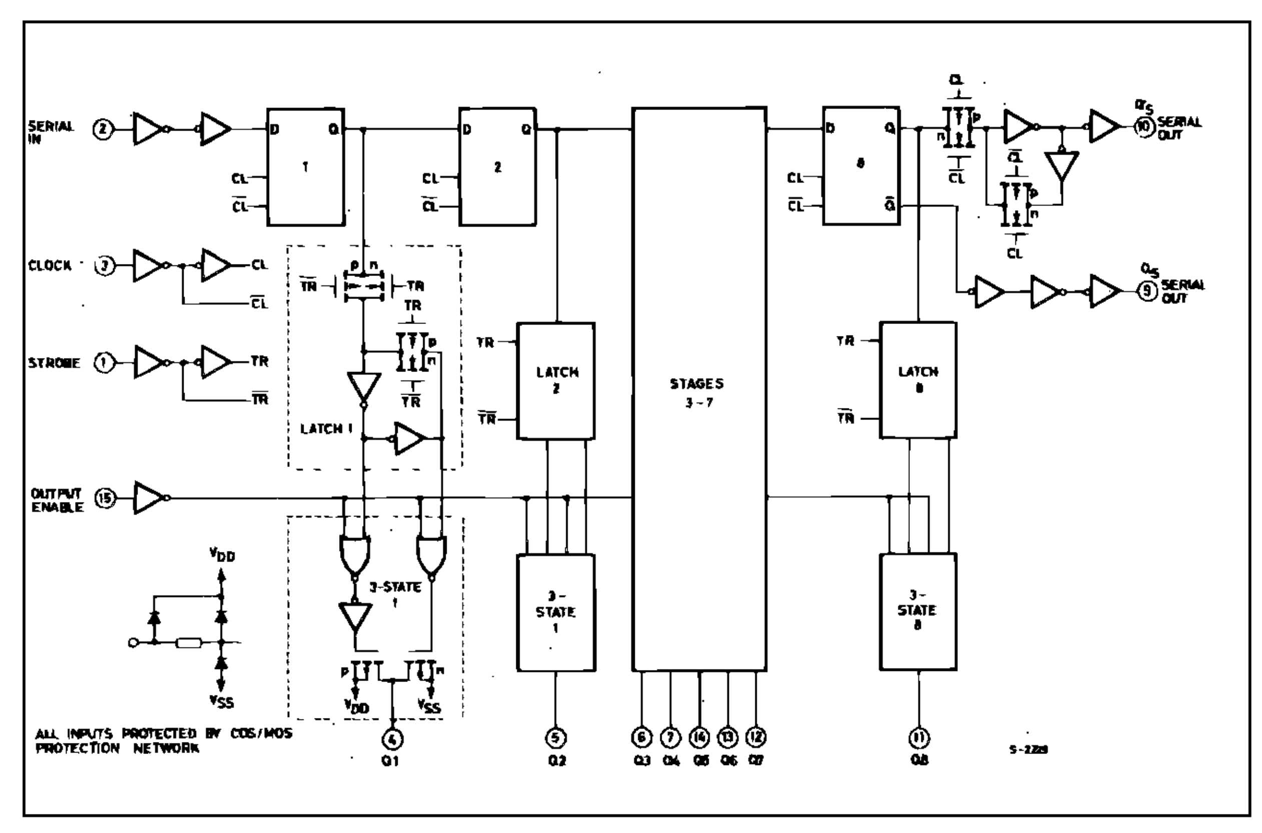
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

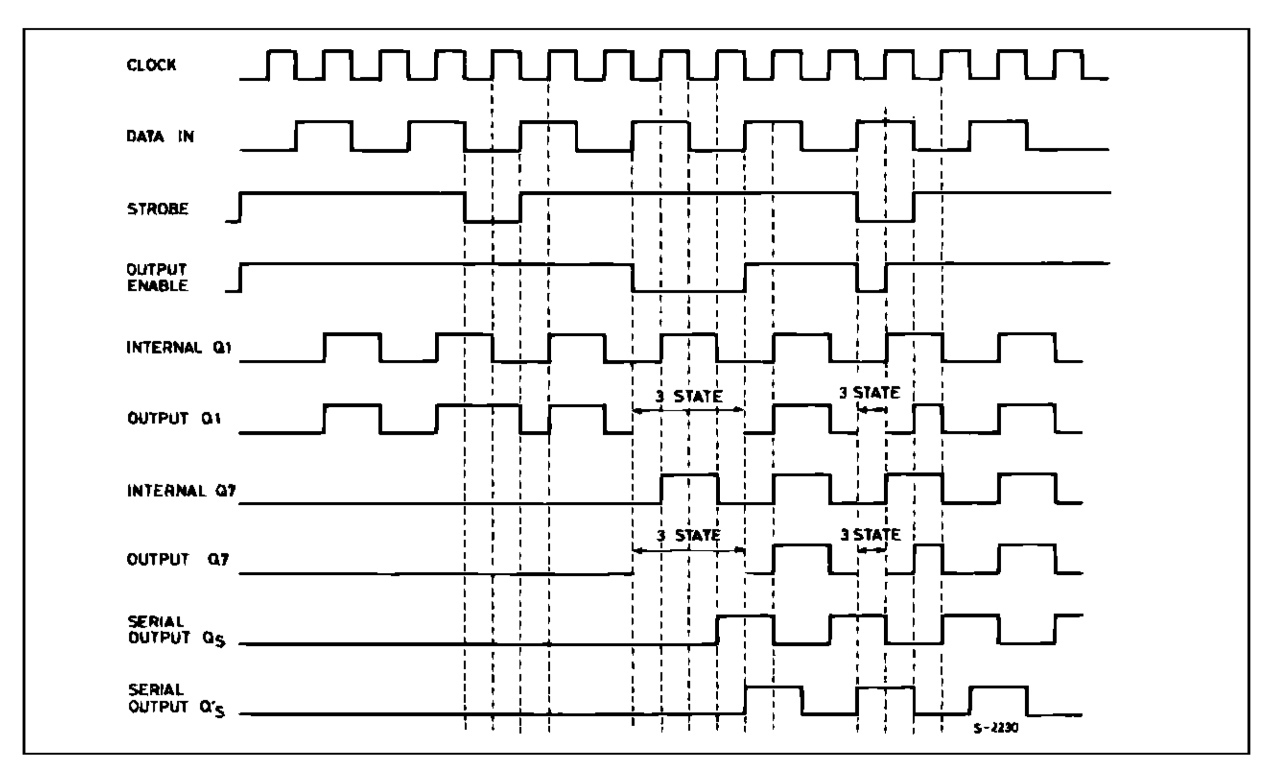
Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage : **HCC** Types **HCF** Types	3 to 18 3 to 15	V V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature : **HCC** Types **HCF** Types	– 55 to + 125 – 40 to + 85	°C °C



LOGIC DIAGRAMS



TIMING DIAGRAM



TRUTH TABLE

TRUTH TABLE

CL$^{\Delta}$	Outputs Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	QN	QS*	Q'S
_/¯	0	X	X	OC	OC	Q7	NC
¯_	0	X	X	OC	OC	NC	Q7
_/¯	1	0	X	NC	NC	Q7	NC
_/¯	1	1	0	0	Q_N-1	Q7	NC
_/¯	1	1	1	1	Q_N-1	Q7	NC
¯_	1	1	1	NC	NC	NC	Q7

▲ = Level Change
X = Don't Care
NC = No Change
OC = Open Circuit

Logic 1 ≡ High
Logic 0 ≡ Low

* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the Q_S output.

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		Test Conditions				Value							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent Current	HCC Types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF Types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output High Voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output Low Voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input High Voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output Drive Current	HCC Types	0/ 5	2.5		5	– 2		– 1.6	– 3.2		– 1.15		mA
			0/ 5	4.6		5	– 0.64		– 0.51	– 1		– 0.36		
			0/10	9.5		10	– 1.6		– 1.3	– 2.6		– 0.9		
			0/15	13.5		15	– 4.2		– 3.4	– 6.8		– 2.4		
		HCF Types	0/ 5	2.5		5	– 1.53		– 1.36	– 3.2		– 1.1		
			0/ 5	4.6		5	– 0.52		– 0.44	– 1		– 0.36		
			0/10	9.5		10	– 1.3		– 1.1	– 2.6		– 0.9		
			0/15	13.5		15	– 3.6		– 3.0	– 6.8		– 2.4		
I_{OL}	Output Sink Current	HCC Types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current	HCC Types	0/18	Any Input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
		HCF Types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	
I_{OH}, I_{OL}	3-state Output Leakage Current	HCC Types	0/18	0/18		18		± 0.4		$\pm 10^{-4}$	± 0.4		± 12	μA
		HCF Types	0/15	0/15		15		± 1.0		$\pm 10^{-4}$	± 1.0		± 7.5	
C_I	Input Capacitance			Any Input						5	7.5			pF

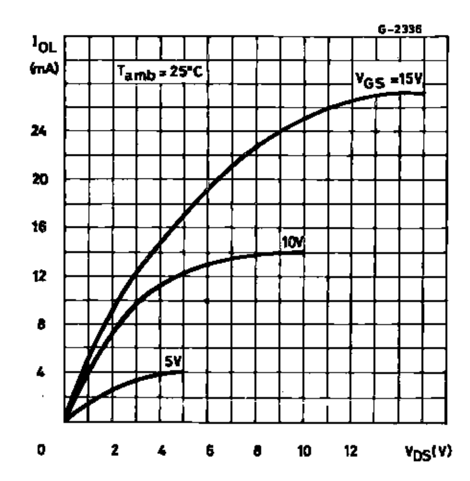
* T_{Low} = – 55°C for **HCC** device : – 40°C for **HCF** device.
* T_{High} = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with V_{DD} = 5V, 2V min. with V_{DD} = 10V, 2.5V min. with V_{DD} = 15V.



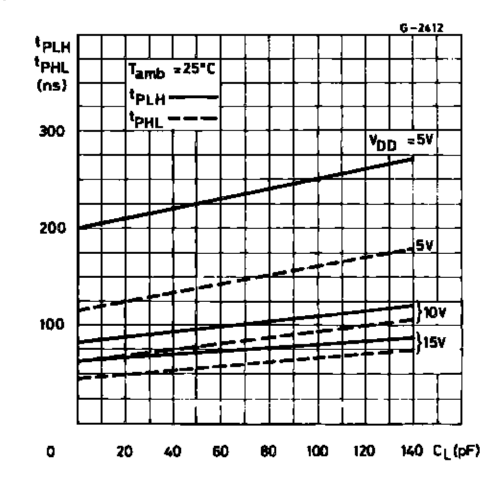
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200kΩ, typical temperature coefficient for all V_{DD} = 0.3%/°C values , all input rise and fall time = 20ns)

Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay Time Clock to Serial Output Q_S		5		300	600	ns
			10		125	250	
			15		95	190	
t_{PLH}, t_{PHL}	Propagation Delay Time Clock to Serial Output Q'_S		5		230	460	ns
			10		110	220	
			15		75	150	
t_{PLH}, t_{PHL}	Propagation Delay Time Clock to Parallel Output		5		420	840	ns
			10		195	390	
			15		135	270	
t_{PLH}, t_{PHL}	Propagation Delay Time Strobe to Parallel Output		5		290	580	ns
			10		145	290	
			15		100	200	
t_{PHZ}	Propagation Delay Time Output Enable to Parallel Output : Output High to High Impedance		5		140	280	ns
			10		75	150	
			15		55	110	
t_{PLZ}	Out Low to High Impedance		5		225	450	ns
			10		95	190	
			15		70	140	
t_W	Strobe Pulse Width		5	200	100		ns
			10	80	40		
			15	70	35		
t_W	Clock Pulse Width		5	200	100		ns
			10	100	50		
			15	83	40		
t_{setup}	Data Setup Time		5	125	60		ns
			10	55	30		
			15	35	20		
t_{TLH}, t_{THL}	Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	
t_r, t_f	Clock Input Rise or Fall Time		5	15			µs
			10	5			
			15	5			
f_{max}	Maximum Clock Input Frequency		5	1.25	2.5		MHz
			10	2.5	5		
			15	3	6		

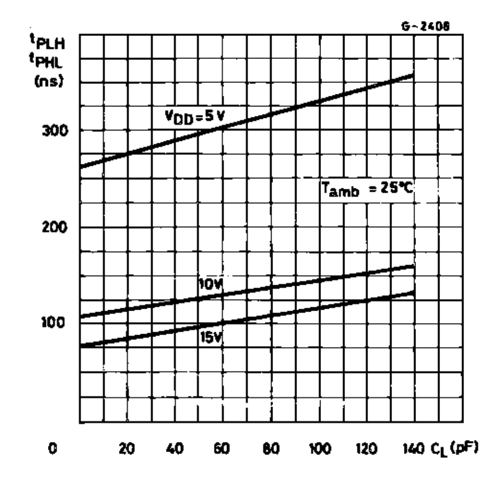
Typical Output Low (sink) Current Characteristics.



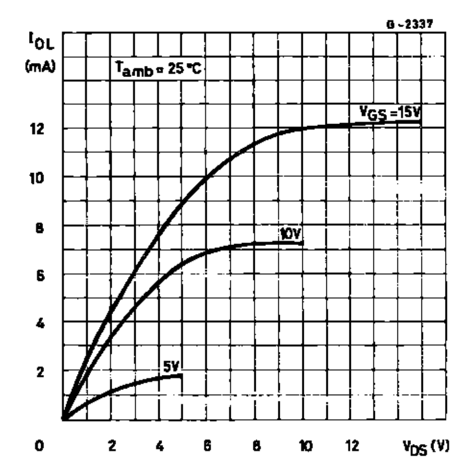
Typical Output High (source) Current Charateris-tics.



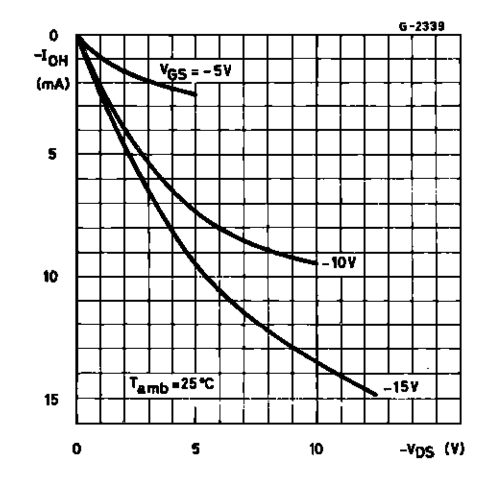
Clock-to-serial Output Q_S Propagation Delay vs. C_L.



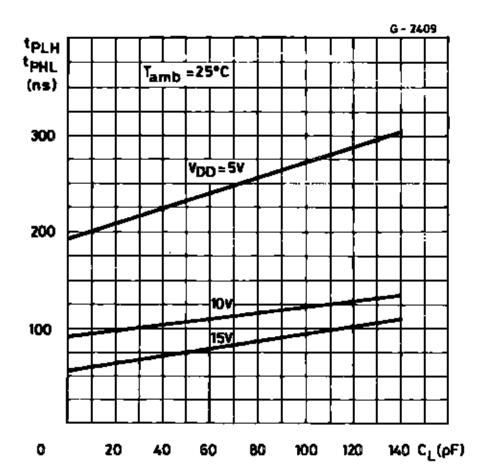
Minimum Output Low (sink) Current Charac-teristics.



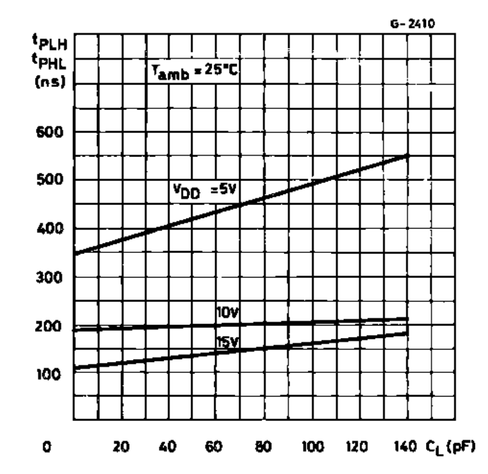
Minimum Output High (source) Current Charac-teristics.



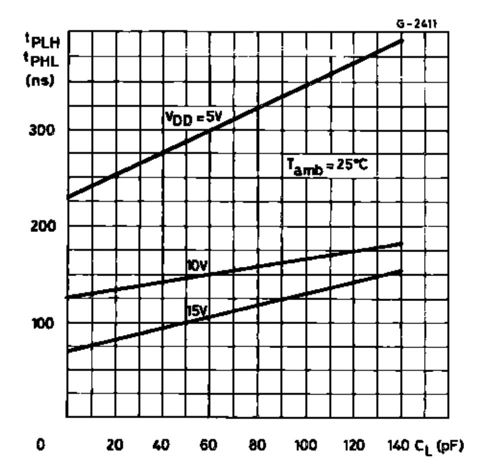
Clock-to-serial Output Q'_S Propagation Delay vs. C_L.



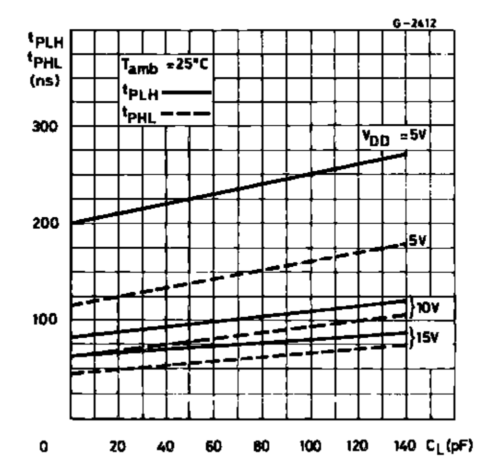
Clock-to-parallel Output Propagation Delay vs. C_L.



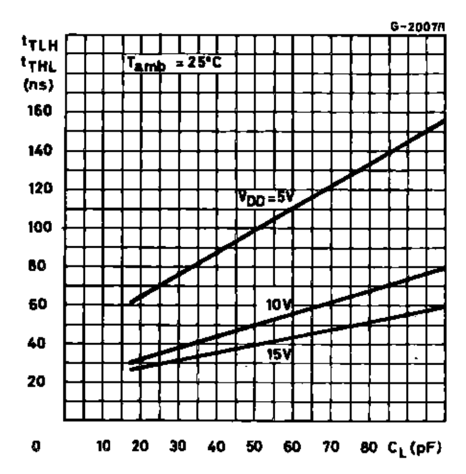
Strobe-to-parallel Output Propagation Delay vs. C_L.



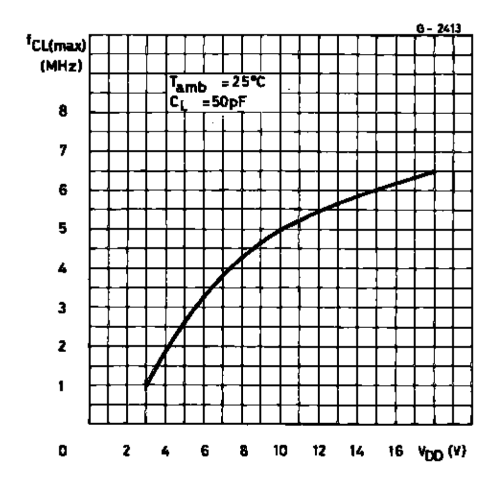
Output Enable-to-parallel Output Propagation Delay vs.



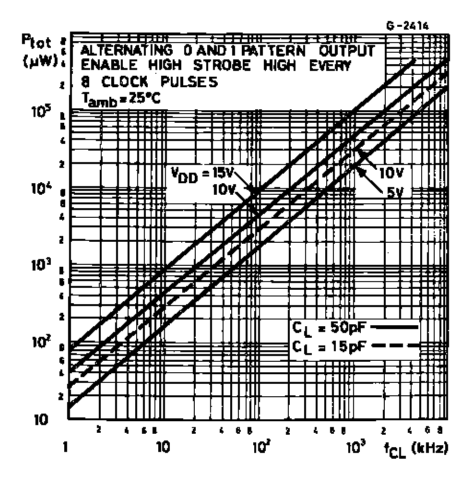
Typical Transition Time vs. Load Capacitance.



Typical Maximum-clock Frequency vs. Supply Voltage.

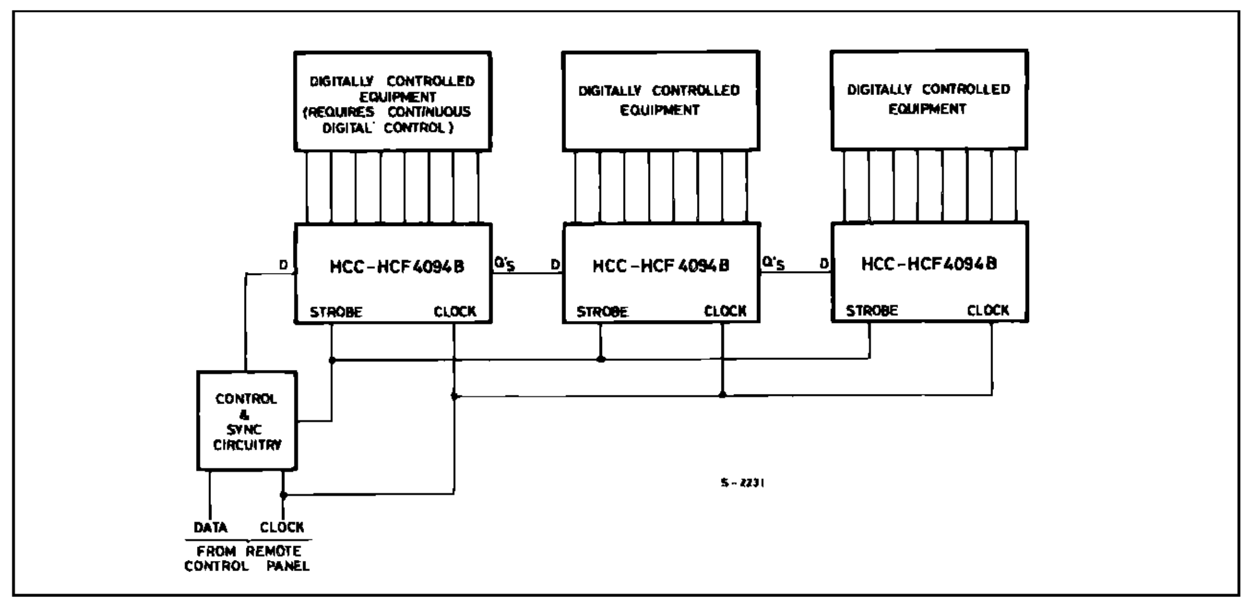


Dynamic Power Dissipation vs. Input Clock Frequency.



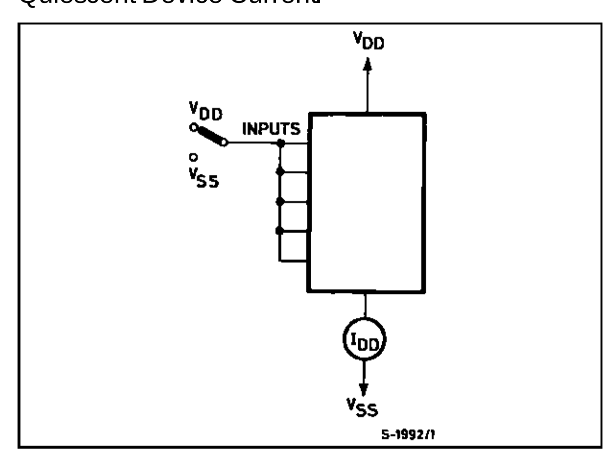
TYPICAL APPLICATION

REMOTE CONTROL HOLDING REGISTER

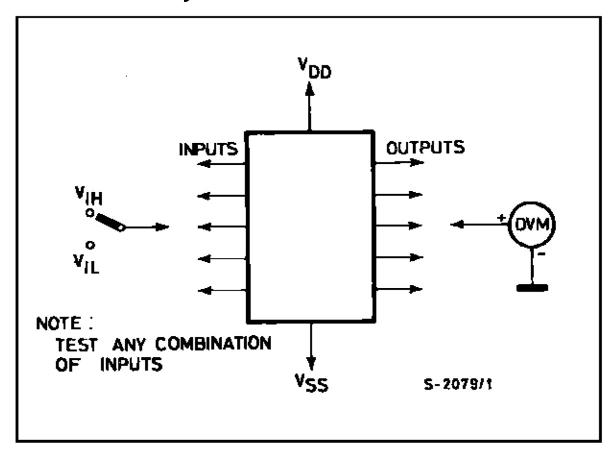


TEST CIRCUITS

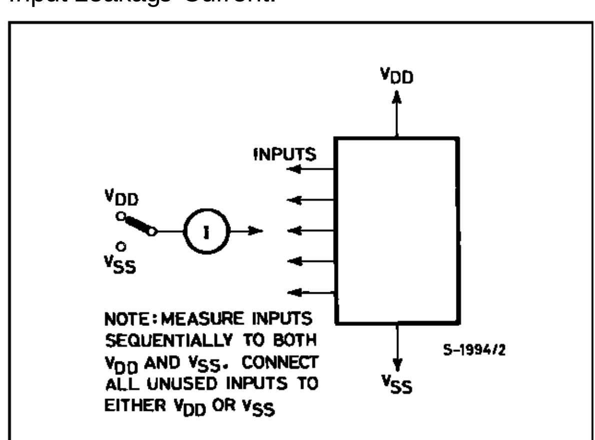
Quiescent Device Current.



Noise Immunity.

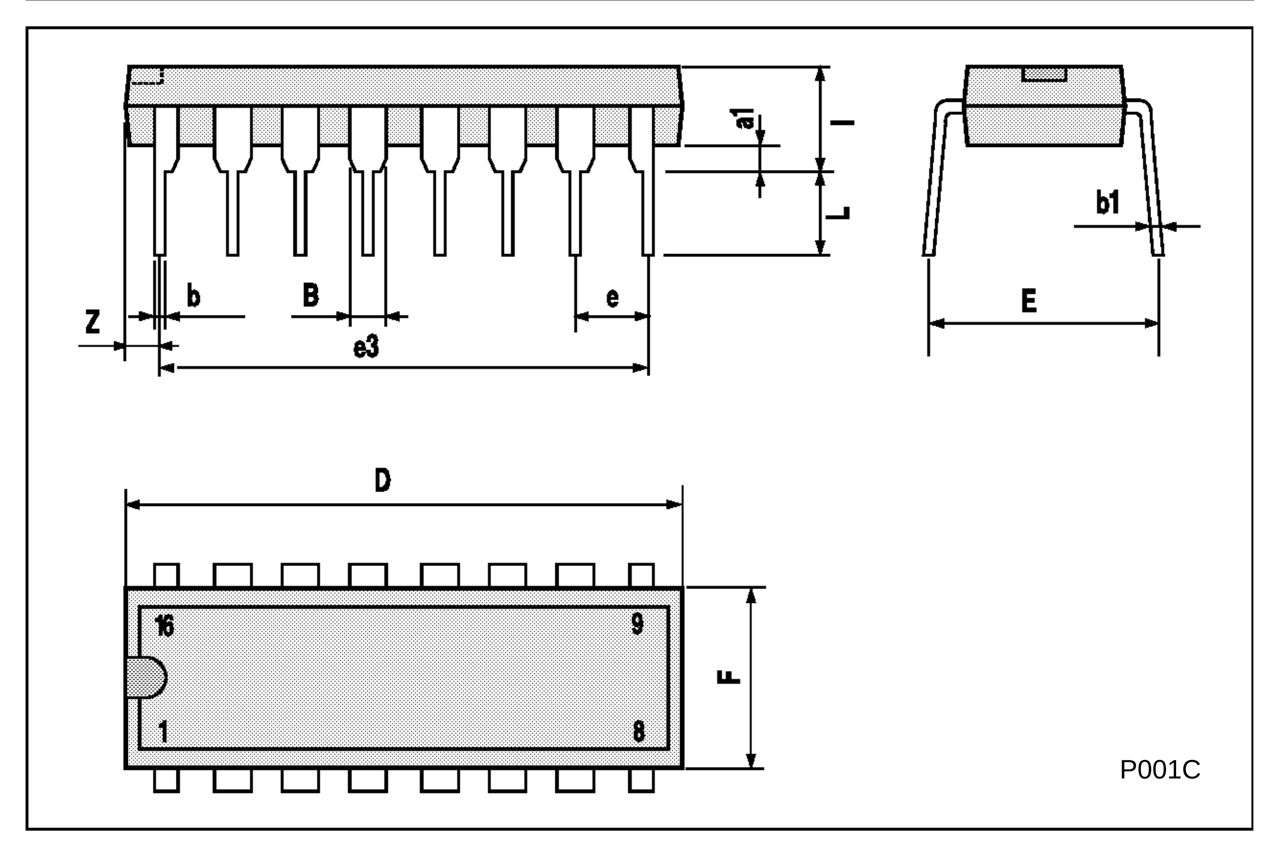


Input Leakage Current.



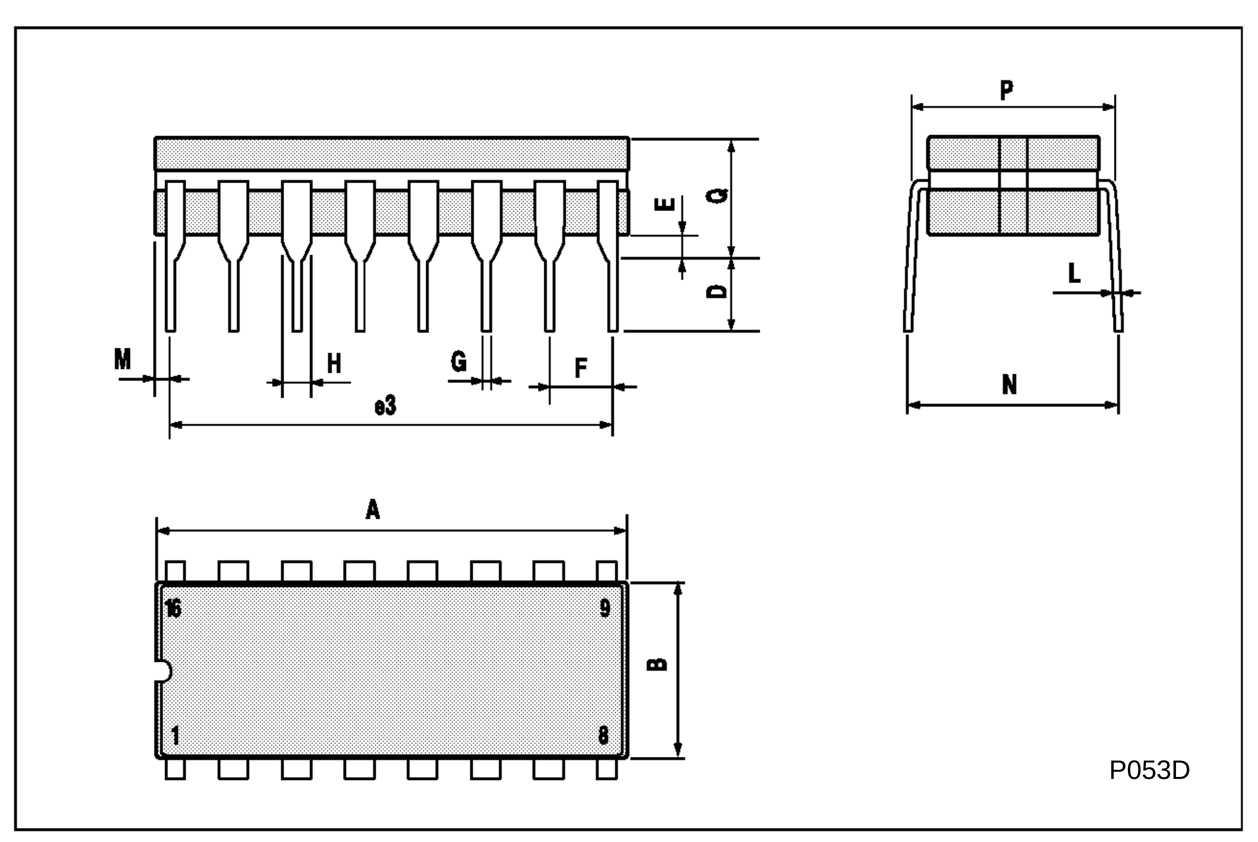
Plastic DIP16 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



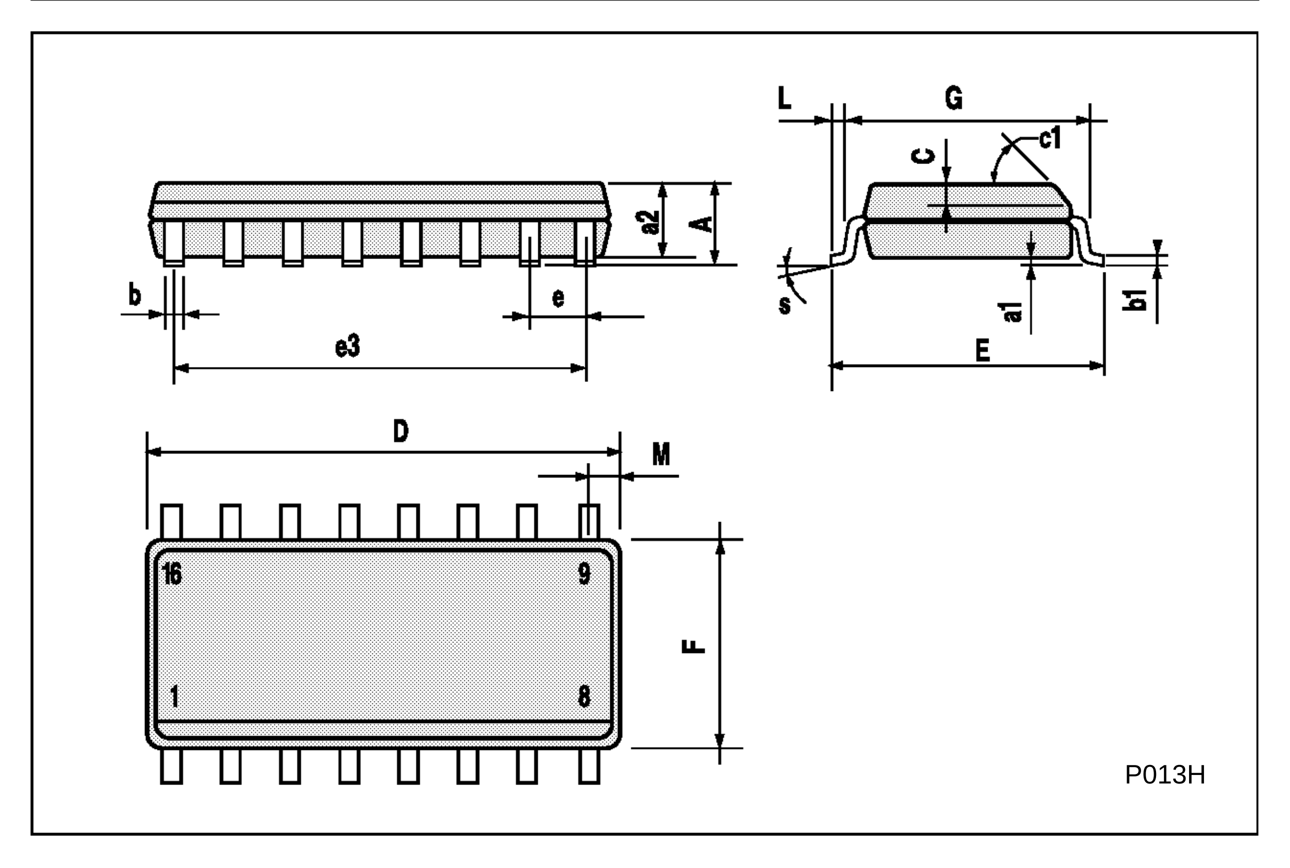
Ceramic DIP16/1 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



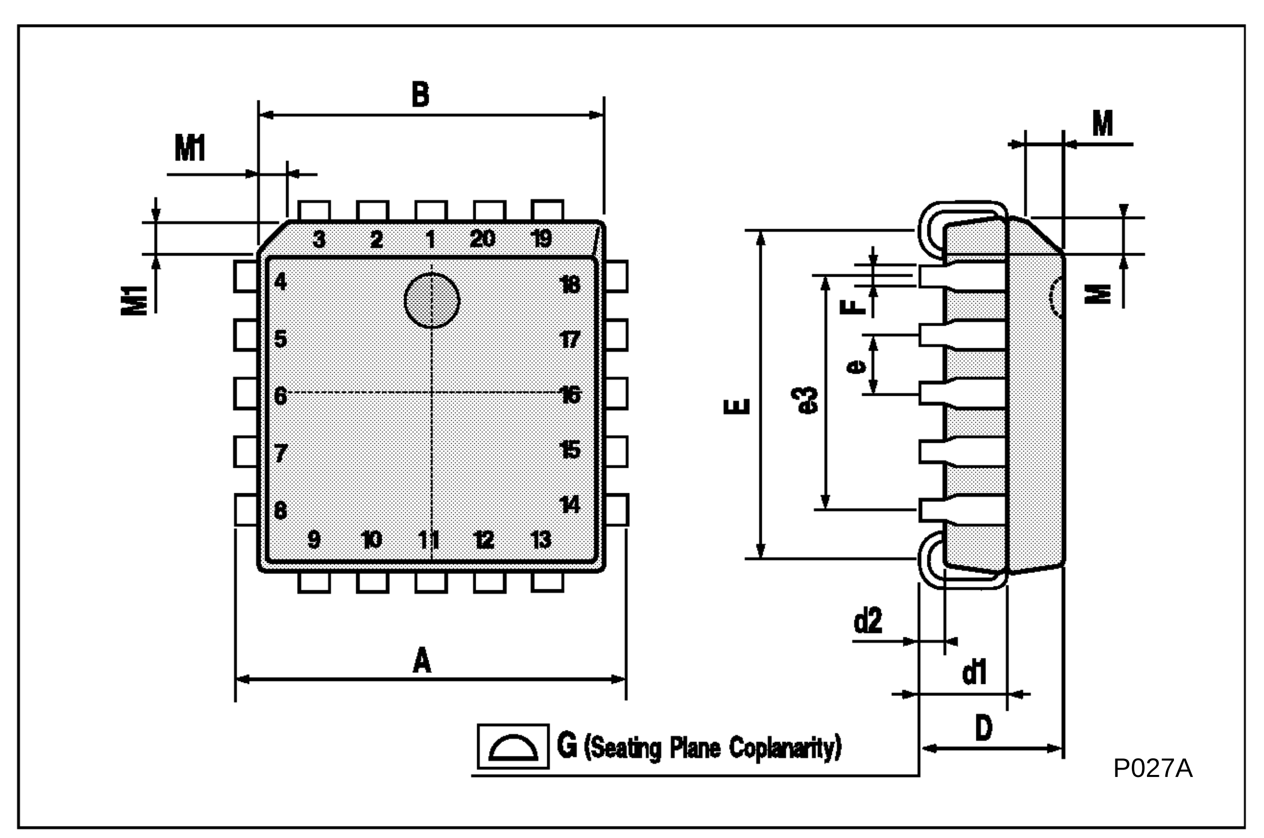
SO16 (Narrow) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	




SGS-THOMSON
MICROELECTRONICS